CLAIMS

1.- A method of manufacturing of a multilayer semiconductor structure comprising a high resistivity silicon substrate with resistivity higher than 3 kΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer, wherein the method comprises suppressing ohmic losses inside the high resistivity silicon substrate by increasing charge trap density between the insulating layer and the silicon substrate.

2.- A method according to claim 1, wherein increasing charge trap density comprises applying an intermediate layer in between the silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm, preferably smaller than 50 nm.

3.- A method according to claim 2, wherein the intermediate layer has a charge trap density of at least $10^{11}/cm^2/eV$, preferably at least $10^{12}/cm^2/eV$.

4.- A method according to any of claims 2 or 3, wherein applying an intermediate layer comprises applying any of an undoped or lightly doped silicon layer, an undoped polysilicon layer, a germanium layer, an undoped polygermanium layer or a poly-SiGe silicon carbide layer in between the silicon substrate and the insulating layer.

5.- A method according to any of claims 2 to 4, the intermediate layer having an RMS roughness, wherein the RMS roughness of the intermediate layer has an average value smaller than or equal to 0.5 nm.

6.- A method according to any of claims 4 or 5, wherein applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer.

7.- A method according to claim 6, wherein crystallizing comprises any of thermal annealing or rapid thermal annealing (RTA) or laser crystallisation.

8.- A method according to any of claims 2 to 7, the method comprising bonding an intermediate layer-covered high resistivity silicon substrate to an insulator-passivated semiconductor substrate.

9.- A method according to claim 8, the method comprising a surface oxidation of the intermediate layer prior to bonding the high resistivity silicon substrate to the insulator-passivated semiconductor substrate.

10.- A method according to any of claims 2 to 7, the method comprising providing an intermediate layer on an insulator-passivated semiconductor substrate, and bonding this to a high-resistivity silicon substrate.

11.- A method according to any of claims 2 to 10, wherein the intermediate layer has a layer thickness of at least 100 nm, preferably between 100 nm and 450 nm, more preferred between 200 nm and 300 nm.

12.- A method according to any of claims 2 to 11, wherein the density of charge traps remains higher than or equal to $10^{11}/cm^2/eV$ after a standard CMOS process is performed on the structure.

13.- A multilayer structure comprising a high resistivity silicon substrate with a resistivity higher than 3 kΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer, wherein the multilayer structure comprises an intermediate layer in between the high resistivity silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm, preferably smaller than 50 nm.

14.- A multilayer structure according to claim 13, wherein the intermediate layer has a trap density of at least $10^{11}/cm^2/eV$, preferably at least $10^{12}/cm^2/eV$.

15.- A multilayer structure according to any of claims 13 or 14, wherein the multilayer structure has an effective resistivity higher than 5 kΩ.cm, preferably higher than 10 kΩ.cm.

16.- A multilayer structure according to any of claims 13 to 15, wherein the intermediate layer comprises any of an undoped or lightly doped silicon layer, an undoped polysilicon layer, a germanium layer, an undoped polygermanium layer or a poly-SiGe silicon carbide layer.

17.- A multilayer structure according to any of claims 13 to 16, wherein the intermediate layer has an RMS roughness with an average value smaller than or equal to 0.5 nm.

18.- A multilayer structure according to any of claims 13 to 17, wherein the active semiconductor layer is made from at least one of Si, Ge, Si_xGe_y, SiC, InP, GaAs or GaN.

19.- A multilayer structure according to any of claims 13 to 18, wherein the insulating layer is formed of at least one of an oxide, a nitride, Si_3N_4, a porous insulating material, a low-k insulating material, a high-k dielectric or a polymer.